AF

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	Dutta et al.	Examiner:	Malzahn, D.
Application No.:	10/005,551	Group Art Unit:	2193
Filed:	November 8, 2001	Docket No.:	US 018181 (VLSI.331PA)
Title:	High-Speed Computation in Arithmetic Logic Circuit		

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence and the papers, as described hereinabove, are being deposited in the United States Postal Service, as first class mail, in an envelope addressed to: Board of Patent Appeals and Interferences, United States Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450, on March 8, 2006.

By: Kelly J. Ledin
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APPEAL BRIEF

Board of Patent Appeals and Interferences
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an Appeal Brief submitted pursuant to 37 C.F.R. § 41.37 for the above-referenced patent application. Please charge Deposit Account No. 50-0996 (VLSI.331PA) in the amount of $500.00 for this brief in support of appeal as indicated in 37 C.F.R. § 41.20(b)(2). If necessary, authority is given to charge/credit deposit account 50-0996 (VLSI.331PA) any additional fees/overages in support of this filing.

I. Real Party in Interest

The real party in interest is the assignee, Koninklijke Philips Electronics, N.V.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-19 are presented for appeal and each of the appealed claims, 1-19, is rejected. Claim 20 has been allowed. The pending claims under appeal may be found in the attached Claims Appendix.

IV. Status of Amendments

No amendments were filed subsequent to the final Office Action dated October 17, 2005.

V. Summary of Claimed Subject Matter

The independent claims involved in the appeal are directed to arrangements and methods for performing binary number arithmetic as a combination of arithmetic operations upon a portion of each binary number and logical operations upon further portions of the binary numbers. This combination reduces the amount of time required to perform binary number arithmetic and improves data throughput.

One example embodiment of the present invention is directed to a circuit arrangement for adding a first binary operand of N bits and a second binary operand of M bits, N being greater than or equal to M. *See, e.g.*, claim 1, Figs.1 and 4, and the corresponding discussions at page 6, line 26 – page 7, line 10 and page 15, line 5 – page 18, line 22. The circuit arrangement includes an adder (*e.g.*, 110a) adapted to add representative sets of least-significant bits of the first and second binary operands together to produce a least-significant bits partial sum and a carryout. The circuit also includes a multiplexer circuit (*e.g.*, 110b of Fig. 1 and 420 of Fig. 4) coupled to the adder and adapted to output a most-significant bits

partial sum by passing one of: a representative set of most-significant bits of the first binary operand, and an offset of the representative set of most-significant bits of the first binary operand, responsive to selection data, the selection data being a function of the most-significant bit of the representative set of least-significant bits of the first binary operand. This circuit arrangement is discussed more specifically in connection with the application of Fig. 4 at page 16, line 4, *et seq*.

Another embodiment of the present invention is directed to a method for adding a first binary operand of N bits and a second binary operand of M bits, N being greater than or equal to M. *See, e.g.*, claim 18, and the corresponding discussion at page 16, line 4 – page 18, line 22. The method includes adding representative sets of least-significant bits of the first and second binary operands together to produce a least-significant bits partial sum and a carryout. The method also includes outputting a most-significant bits partial sum by passing one of: a representative set of most-significant bits of the first binary operand, and an offset of the representative set of most-significant bits of the first binary operand. The output is responsive to selection data, the selection data being a function of the most-significant bit of the representative set of least-significant bits of the first binary operand. The discussion at page 16, line 13 – page 18, line 22 includes several examples in which the claimed method is applicable.

Another embodiment is directed to a circuit arrangement for adding a first binary operand of N bits and a second binary operand of M bits, N being greater than or equal to M. *See, e.g.*, claim 19, Figs.1 and 4, and the corresponding discussions at page 6, line 26 – page 7, line 10 and page 15, line 5 – page 18, line 22. The arrangement includes means for adding representative sets of least-significant bits of the first and second binary operands together to produce a least-significant bits partial sum and a carryout (*e.g.*, 110a of FIG. 1, an adder, a second binary operand (M)-bit adder). The arrangement further includes means for outputting a most-significant bits partial sum (*e.g.*, 110b of FIG. 1, a multiplexer, a 4x1 multiplexer, logic circuitry, an XOR gate, a multiplexer implementing an XOR function) by passing one of: a representative set of most-significant bits of the first binary operand, and an offset of the representative set of most-significant bits of the first binary operand, responsive to selection data, the selection data being a function of the most-significant bit of the representative set of least-significant bits of the first binary operand.

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

VI. Grounds of Rejection to be Reviewed on Appeal

A. Claims 1-19 are rejected under 35 U.S.C. § 112(2).

B. Claims 1-19 are rejected under 35 U.S.C. § 102(b) over Daniels *et al.* (U.S. Patent No. 4,203,157).

VII. Argument

A. The Section 112(2) rejection of claims 1-19 is improper because the Examiner fails to present a proper Section 112 rationale as Section 112(2) does not require that the claim(s) cover only operable embodiments.

Section 112(2) requires that the claims particularly point out and distinctly claim the subject matter of the invention. The Examiner's assertion that claim 1 is mis-descriptive according to one example implementation discussed in the Specification is not a requirement of Section 112(2) or any other paragraph of Section 112. The Examiner's assertion regarding the alleged inoperability of a single claimed combination, even if correct, is not a proper basis for a Section 112 rejection. *See, e.g., In re Dinh-Nguyen*, 492 F.2d 856, 858-59, 181 USPQ 46, 48 (CCPA 1974) (stating that a claim is not necessarily invalid even if some of the claimed combinations are inoperative). The Examiner's arguments acknowledge that the instant claims are particular and distinct as the Examiner was able to ascertain a specific embodiment from the claim language. Moreover, several operable embodiments are covered by claim 1 such as are discussed at page 15, line 5 – page 18, line 22. Accordingly, Appellant submits that the claim language complies with Section 112(2), and the premise underlying the Section 112 rejection is not supported by the law. Appellant accordingly requests that the rejection be withdrawn.

More specifically, the Examiner uses independent claims 1 to argue that (i) N needs to be greater than M if the multiplexer outputs a most significant bits (MSBs) partial sum and (ii) that the selection data is a function of the MSB of the set of least-significant bits (LSBs) of the second, not first, binary operand. Thus, it would appear that the Examiner questions whether N can be equal to M.

First, Appellant submits that N need not necessarily be greater than M because the claimed invention permits this configuration, N equal to M, as set forth, for example, in claim 1. Thus, by definition, the scope of the claimed invention permits for this situation.

Second, the Examiner is incorrect in arguing that N must be greater than M if the multiplexer outputs an MSB partial sum. The Examiner's assertion (that where "N=M then N – M = 0 and there is not partial sum") assumes that where N equals M, a representative set of MSBs cannot exist. This argument carries the erroneous rationale that assumes partial sums cannot be performed on operands of equal bits. By maintaining this argument, the Examiner fails to recognize that the multiplexer can output a MSB partial sum whether N is greater than M, or N is equal to M. This situation can arise, for example, because the multiplexer can output an MSB partial sum whenever the multiplexer passes "a representative set of most-significant bits of the first binary operand," as set forth in claim 1. Put another way, the multiplexer output of an MSB partial sum is not precluded when N equals M because it can still be supplied as a representative set of most-significant bits. Consider, for example, a situation where N and M are both equal to eight; an MSB partial sum of the bits four to seven could be taken. Moreover, the MSB and LSB sets are not claimed to be mutually exclusive, allowing for LSB and MSB sets to potentially contain some of the same bits. Accordingly, the first-mentioned rationale "(i)" is incorrect.

The Examiner also erroneously argues that (ii) the selection data is a function of the MSB of the set of LSBs of the second, not the first, binary operand. This is incorrect as the claimed aspect of the invention is supported, for instance, in the Specification at page 6, lines 5-13 (particularly the clause at page 6 lines 22-23). The Examiner asserts that Equation B, illustrated by Fig. 3 and implemented in Fig. 4, shows that the first operand is not used for the selection of the multiplexer output. The Examiner's assertion fails to note that Fig. 3 and Fig. 4 also show selection bit C15. Appellant submits that C15 is a function of the MSB of the set of LSBs of the first binary operand. Moreover, the Specification at page 15, line 5, describes Fig. 4 as "one example" and further describes Fig. 3 as "an example" at page 5, line 1. Accordingly, the second-mentioned rationale "(ii)" is incorrect.

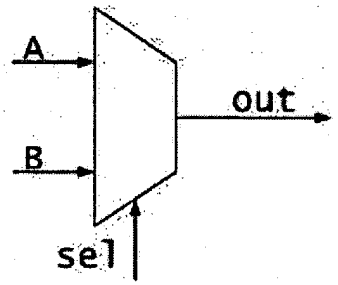
Claims 16 & 17

With respect to dependent claims 16 and 17, the Examiner asserts that the claimed digital filtering circuit arrangement is inconsistent with claim 1 because claim 1 is "limited to a

circuit arrangement for adding." Appellant notes that claim 1 is directed to a circuit arrangement that includes an adder and a multiplexer circuit and is in no way limited to an adder circuit. As discussed in detail in the instant Specification, the arrangement of claim 1 is available for implementation as a digital filtering arrangement, and Appellant accordingly requests that the rejection be reversed.

B. The rejection of claims 1-19 is improper because the Examiner fails to present correspondence between the cited '157 reference and each of the claimed limitations.

The '157 reference is largely unrelated to the claimed invention, and the Examiner fails to identify where the '157 reference teaches basic claim limitations of Appellant's invention including, for example, a multiplexer that provides the claimed output in response to selection data, by passing the claimed inputs. In digital circuit design, a multiplexer is a device that has multiple input streams and only one output stream. It forwards one of the input streams to the output stream based on the values of one or more "selection inputs." *See, e.g.*, www.wikipedia.com. An example visual representation of these multiple inputs and single output to a multiplexer device is shown below.



In the above representation, "sel" is selection data which is an input along with the "A" and "B" streams. In an attempt to assert correspondence, the Examiner alludes to circuitry of the '157 reference "that selectively outputs the result as either the output of the increment/decrement network or the output of the temporary register;" however, this unidentified circuitry is not a multiplexer. The '157 Abstract indicates that the two possible outputs are located in two different locations: 1) output of the increment/decrement network, and 2) output of the temporary register. Thus, the Examiner fails to identify a single circuit that receives both possible outputs and selection data for determining the output of the result.

A word search of the '157 reference confirms that the term "multiplexer" is not used in the '157 reference.

The Examiner also fails to identify how the alleged circuitry corresponds to the claimed multiplexer. More specifically, the Examiner fails to identify any selection data being a function of the most-significant bit of the representative set of least-significant bits of the first binary operand. The relied-upon teachings, specifically the Abstract of the '157 reference, fails to teach such selection data. The Abstract states that "The carry signal and the sign bit of the 8-bit operand control the mode of operation of the increment/decrement network and determine whether the increment/decrement network or the temporary register will be selected to provide the most significant byte of the result." Thus, according to the '157 Abstract, the alleged selection data is a function of the sign bit of the second binary operand, not the first, as claimed.

When applying the '157 teachings to claim 1, for example, the first binary operand has N bits and the second operand has M bits where N must be equal to or greater than M. Therefore the first operand of the '157 reference is 16 bits and the second operand is 8 bits. Thus, "the sign bit of the 8-bit operand" fails to correspond to the claimed selection data because it is a function of the second binary operand (the 8-bit operand).

Moreover, the Examiner fails to assert or identify any correspondence between any of the dependent claims and the '157 reference. For example, no correspondence is asserted to: N being 24 and M being 16(claim 4); a multiplexer adapted to select one of at least three input binary quantities (claim 7); multiplexer circuit configured to operate as an exclusive-or gate (claim 11); both operands being unsigned binary numbers (claim 15); and a digital filtering arrangement (claim 16). Appellant fails to recognize where the '157 reference teaches any of these, and other, dependent claim limitations.

Without a presentation of correspondence to each of the claimed limitations, the Section 102(b) rejection is improper. Appellant accordingly requests that the rejection be reversed.

VIII. Conclusion

In view of the above, Appellant submits that the rejections are improper, the claimed invention is patentable, and that the rejections of claims 1-19 should be reversed. Appellant

respectfully requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

Should there be any issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Mr. Peter Zawilski, of Philips Corporation at (408) 474-9063.

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CLAIMS APPENDIX

1. A circuit arrangement for adding a first binary operand of N bits and a second binary operand of M bits, N being greater than or equal to M, comprising:

an adder adapted to add representative sets of least-significant bits of the first and second binary operands together to produce a least-significant bits partial sum and a carryout; and

a multiplexer circuit coupled to the adder and adapted to output a most-significant bits partial sum by passing one of: a representative set of most-significant bits of the first binary operand, and an offset of the representative set of most-significant bits of the first binary operand, responsive to selection data, the selection data being a function of the most-significant bit of the representative set of least-significant bits of the first binary operand.

2. The circuit arrangement of claim 1, wherein the adder is an M-bit adder, the representative sets of least-significant bits of the first and second binary operands each have a length of M bits, and the selection data includes a carryout from the M-bit adder, and the Mth bit of the first binary operand.

3. The circuit arrangement of claim 2, wherein the most-significant bits partial sum is one of: N-M most significant bits of the first binary operand, N-M most significant bits of the first binary operand incremented by one, and N-M most significant bits of the first binary operand decremented by one.

4. The circuit arrangement of claim 3, wherein N is 24 and M is 16.

5. The circuit arrangement of claim 1, wherein the offset of the representative set of most-significant bits of the first binary operand include a first incremented offset, and a second decremented offset.

6. The circuit arrangement of claim 5, wherein the first incremented offset is the representative set of most-significant bits of the first binary operand incremented by one, and

the second incremented offset is the representative set of most-significant bits of the first binary operand decremented by one.

7. The circuit arrangement of claim 6, wherein the multiplexer circuit includes a multiplexer adapted to select one of at least three input binary quantities.

8. The circuit arrangement of claim 1, wherein the selection data includes the most-significant bit of the representative set of least-significant bits of the first binary operand, and a carryout from the adder.

9. The circuit arrangement of claim 8, wherein the carryout is available from the adder before the least-significant bits partial sum.

10. The circuit arrangement of claim 1, wherein the offset of the representative set of most-significant bits of the first binary operand include a first incremented offset, and a second decremented offset, wherein the first incremented offset is the representative set of most-significant bits of the first binary operand incremented by one, and the second incremented offset is the representative set of most-significant bits of the first binary operand decremented by one, wherein the selection data includes the most-significant bit of the representative set of least-significant bits of the first binary operand, and a carryout from the adder, and wherein the carryout is available from the adder before the least-significant bits partial sum.

11. The circuit arrangement of claim 1, wherein N-M is one, and the multiplexer circuit is further configured to operate as an exclusive-or gate, the selection data being the most-significant bit of one of the representative sets of the first binary operand and a carryout from the adder.

12. The circuit arrangement of claim 1, wherein N equals M, the most-significant bit of the second binary operand is zero, and the multiplexer circuit is further configured to operate

as an exclusive-or gate, the selection data being the most-significant bit of one of the representative sets of the first binary operand and a carryout from the adder.

13. The circuit arrangement of claim 12, wherein the carryout is available from the adder before the least-significant bits partial sum.

14. The circuit arrangement of claim 1, wherein the operands are unsigned binary numbers, and the multiplexer circuit is further configured to operate as an exclusive-or gate, the selection data being the most-significant bit of the first binary operand and a carryout from the adder.

15. The circuit arrangement of claim 1, wherein the operands are unsigned binary numbers.

16. A digital filtering circuit arrangement, according to claim 1, wherein the adder and the multiplexer are part of a pipelined datapath unit.

17. The digital filtering circuit arrangement of claim 16, further including a processor and a memory, wherein the processor feeds data through memory to the pipelined datapath unit.

18. A method for adding a first binary operand of N bits and a second binary operand of M bits, N being greater than or equal to M, comprising:

adding representative sets of least-significant bits of the first and second binary operands together to produce a least-significant bits partial sum and a carryout; and

outputting a most-significant bits partial sum by passing one of: a representative set of most-significant bits of the first binary operand, and an offset of the representative set of most-significant bits of the first binary operand, responsive to selection data, the selection data being a function of the most-significant bit of the representative set of least-significant bits of the first binary operand.

19. A circuit arrangement for adding a first binary operand of N bits and a second binary operand of M bits, N being greater than or equal to M, comprising:

means for adding representative sets of least-significant bits of the first and second binary operands together to produce a least-significant bits partial sum and a carryout; and

means for outputting a most-significant bits partial sum by passing one of: a representative set of most-significant bits of the first binary operand, and an offset of the representative set of most-significant bits of the first binary operand, responsive to selection data, the selection data being a function of the most-significant bit of the representative set of least-significant bits of the first binary operand.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.